UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,750	01/14/2004	Christopher A. Menkus	08211/0200349-US0/P05782	4265

38845 7590 08/15/2005

DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,750	MENKUS, CHRISTOPHER A.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,14-17,19 and 21-25* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 8/10/05. Claims 18 and 20 have been canceled. Claims 1 – 17, 19 and 21 - 25 are pending on this application.

Response to Amendment

2. Applicant's amendment has overcome the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. However, a new ground of non-final rejection is applying in this office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 9, 14 – 17, 19, and 21 - 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. U.S. Patent No. 6,535,156 in view of Lee et al. and further view of Chen et al. U.S. Patent No. 6,628,216.

Regarding claim 1, Fig. 1 of Wang et al. discloses an analog-to-digital conversion converter comprising: a fine channel circuit (202) that includes folding stages (Col. 2 lines 8 – 13); a coarse channel circuit (203) with adjustment circuit (321). However, Wang et al. does not disclose a coarse channel calibration circuit; wherein the coarse

channel calibration circuit includes a counter circuit coupled to the adjustment circuit (312).

Fig. 3 of Lee et al. discloses an analog-to-digital converter circuit 305 comprising: coarse channel calibration circuit (304) and fine channel adjustment circuit (302).

Fig. 8 of Chen et al. disclosing a calibration circuit (Col. 16 lines 52 – 61) for analog to digital converter (Fig. 1 [100]); wherein the coarse channel calibration circuit (Fig. 8) includes a counter circuit (809) and a parameter adjustment circuit (811) that is couple to the counter circuit (809).

Wang et al., Lee et al. and Chen et al. are common subject matter for analog to digital converter. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the coarse calibration of Lee et al. into the coarse channel of Wang et al. for the purpose of providing adjusting offset of input signal and adjust signal gain such that the full dynamic range of system is utilized (Lee et al., Col. 3 lines 14 – 28); and further incorporated the counter of calibration circuit taught by Chen et al. into the calibration of Wang/Lee for the purpose of providing a predetermined internal to generated the sum value of the output stream bits (Chen et al.; Col. 18 lines 18 – 24).

Regarding claim 2, Fig. 8 of Chen et al. further comprising: a control circuit (807) that is configured to provide a select signal (801); and a voltage reference circuit (139) that is configured to provide a voltage reference signal (output of 13) that corresponds to the select signal (output of 807), wherein the coarse channel circuit (805; See Col. 18 lines 18 - 21) is configured to receive the voltage reference signal

Regarding claim 3, Fig. 8 of Chen et al. further discloses wherein the coarse channel circuit (805) is configured to provide an output signal (output of 805) in response to a voltage reference signal (139), and wherein the coarse channel calibration circuit (805) is configured to: receive a feedback signal (Output of output of 805) from the coarse channel circuit (Fig. 8), and provide an adjustment signal (output of 811) to the coarse channel circuit in response to the feedback signal (Col. 4 line 64 – Col. 5 line 9).

Regarding claim 4, combination of Wang, Lee and Chen et al. as applied to claim 1 above, further discloses wherein the coarse channel circuit (Chen et al. Fig. 6) comprises an amplifier array (PA) and a comparator array (C0...C13) wherein at least one the amplifier array or comparator array is configured to received an adjustment signal (Chen et al. Fig. 1[134, 135])

Regarding claim 5, the claim incorporated similar subject matter feedback signal as of claim 3, and rejected along the same rationale.

Regarding claim 6, the claim incorporated similar subject matter as of claim 1, and is rejected along the same rationale.

Regarding claim 7, Fig. 3 of Lee et al. as applied to claim 1 above further discloses wherein the adjustment circuit (302) includes a DAC (312) to provide a converted signal (output of 312) to the coarse channel signal.

Regarding claim 8, Wang, Lee and Chen et al. as applied to claim 1 above, and (Fig. 8) of Chen et al. further discloses a feedback signal (BitS), the counter circuit (809) received the feedback signal (BitS), the parameter adjustment circuit (811) receive the

count signal (SUM) and adjustment parameter (output of 811) response to the count signal (SUM).

Regarding claim 9, Chen et al. as applied to claim 8 above, further discloses wherein the parameter comprises one single-ended current or differential current (Chen et al., Col. 26 lines 10 – 13).

Regarding claim 14, Wang, Lee and Chen et al. as applied to claim 1 above, and (Fig. 8) of Chen et al. further disclose a control circuit (807) providing a selecting signal (output of 807); a timing signal (CLK); and the calibration circuit (Fig. 8) is configured to latch the output (BitS) response to the timing signal (CLK).

Regarding claim 15, the claim incorporated similar subject matter as of claims 1 and 8, and rejected along the same rationale.

Regarding claim 16, Wang, Lee and Chen et al. as applied to claim 1 above, and (Fig. 8) of Chen et al. further disclose a control circuit (807) provide a selecting signal (output of 807) for selecting a voltage reference (139) and assert a timing signal (CLK) for latching the circuit at a predetermined amount of time after a change of the selection signal (output of 807).

Regarding claim 17, the claim incorporated similar subject matter as of claim 1, and rejected along the same rationale.

Regarding claim 19, Wang, Lee and Chen et al. as applied to claim 1 above, and (Fig. 8) of Chen et al. further disclose a reference voltage (319) and adjusting parameter (811) of the coarse channel circuit (Col. 16 lines 59 – 61) until an output put of coarse channel circuit is calibrated in relation to the reference voltage (Col. 16 lines 59 – 61);

receiving a signal from the channel circuit (BitS) after providing the reference voltage (T1 – T7) and adjusting a count (809) in response to the signal (BitS), wherein the parameter is adjusted according to the count.

Regarding claim 21, Wang, Lee and Chen et al. as applied to claim 1 above, and (Fig. 1) of Wang et al. further discloses wherein the coarse channel circuit (201) is arranged to perform analog-to-digital conversion of the input signal (206) in parallel with fine analog to digital converter (201).

Regarding claim 22, the claim incorporated similar subject matter as of claim 14 and rejected along the same rationale.

Regarding claim 23, the claim incorporated similar subject matter as of claim 4 and rejected along the same rational.

Regarding claim 24, the claim incorporated similar subject matter as of claim 3, and rejected along the same rationale.

Regarding claim 25 the claim incorporated similar subject matter as of claim 21 and rejected along the same rationale.

Allowable Subject Matter

5. Claims 10 - 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 10, prior arts fail to teach a folding Analog-to-Digital converter comprising a counter circuit is configured to, if latched: increment a count

value that is associated with the count signal if the comparator output response to a first level, and decrement the count value if the comparator output response to a second logic level.

With respect to claim 11, prior art fails to teach wherein the parameter adjustment circuit includes a first digital-to-analog converter circuit that is configured to convert the count signal into a first analog signal; and a second digital-to-analog converter circuit that is configured to convert an inverted count signal into a second analog signal.

Cited References

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references are relating to coarse and fine analog-to-digital converter.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are

(703-872-9306) for regular communications and (703-872-9306) for After Final communications.

8/12/05

Linh Van Nguyen

Art Unit 2819